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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2685	

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15

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/721,528	Applicant(s) LUFF ET AL.	
	Examiner Lana N Le	Art Unit 2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,20-25 and 31-42* is/are rejected.

7)☒ Claim(s) *1-5,7-19 and 26-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-5, 7-8, 13-14*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDSs) submitted on 05/14/01, 06/18/01, 10/03/01, 02/12/02, 03/15/04, and 06/18/04. The information disclosure statements have been received and placed of record in the file and are considered by the examiner.

Priority

2. Acknowledgement is made of applicant's claim for priority under 35 U.S.C. 119 (e) of copending U.S. provisional application number 60/167,188.

Preliminary Amendments

3. The preliminary amendment filed on 06/26/02, 09/09/02, and 10/18/02 have been received and placed of record in the file.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Therefore, the second capacitor and third capacitor of dependent claim 15, lines 9-15, if not a mistake to be the same as the first and second cascode capacitor of independent claim 14 lines 12-18, must be shown or the feature(s) canceled from the claim(s); and if it is a mistake in which the second and third capacitor of claim 15 at lines 9-15 are the same as the first and second cascode capacitor of independent claim 14

lines 12-18, the second and third capacitor of claim 15 at lines 9-15 should be deleted and if they are deleted, --fourth capacitor--- at line 28 and line 31 of claim 15 should be --third cascode capacitor--- and ---fifth capacitor--- at line 31 of claim 15 should be ---fourth cascode capacitor----, and claim 16 line 9 --sixth capacitor-- should be -second capacitor--- due to it not being a cascode capacitor.

Also the sixth capacitor of claim 16, lines 9-10, must be shown or the feature(s) canceled from the claim(s).

No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1, 6-21 and 26-34 are objected to because of the following informalities:

Regarding claim 31, it should be renumbered as claim 30 since there is no claim 30.

Regarding claim 1, line 10, ---control terminal-- should be ---first terminal---;

at line 15, ---second--- should be ---third---;

at line 17, ---second--- should be ---third---;

at line 20, ---third--- should be --second--;

Regarding claim 6,

at line 8, --the RF input circuit---- should be ---the low noise RF input circuit---;

Regarding claim 7, at line 1, "A mixer" should be "The mixer circuit";

at line 3, --a third inductor--- should be ----a first inductor---;

at line 7, --first terminal--- should be ---first terminal,----;

at line 10, --a second terminal of the--- should be --the second terminal of the----;

at line 15, ---a second biasing--- should be --- a first biasing---;

at line 16, ---a second bias--- should be --- a first bias---.

Regarding claim 8, at line 1, --A mixer--- should be ---The mixer circuit----; --a RF--- should be ---an RF---;

at line 3, --the supply-- should be ---a supply---;

at line 4, ---the first input transistor--- should be ---the first transistor---;

--- to correspond with "a first transistor" of claim 7 line 7;

at line 5, ---the first terminal of the supply resistor--should be ---a first terminal of a supply resistor---, ---and to the first---- should be ---and to a first----;

at line 7, --the base-- should be --a base---;

at line 8, ---input transistor--- should be! ---transistor---;

at line 9, ---a second--- should be ---a fourth---- and ----second terminal--- should be --first terminal---;

Regarding claim 9, at line 1, --A mixer--- should be ---The mixer circuit----;

at line 7, ---a third resistor--- should be ---a first resistor----;

at line 10, ---third---- should be ----first-.---;

at line 11, ---the third---- should be ---the first----;

at line 13, ---the ground--- should be ---a ground---;

at line 14, ---fourth resistor--- should be ---second resistor---;

at line 16, ---second transistor--- should be ---first transistor---;

at line 17, --and--- should be --and an---;

at line 17, ---fourth resistor--- should be ---second resistor---;

at line 18, ---third transistor--- should be ---second transistor---;

at line 21, --fifth-- should be ---third---;

at line 22, a comma is missing after ---transistor---;

at line 24, ---second-- should be ---first-- and ---third--- should be ---second---;

at line 27, --fifth-- should be -third--, and --third-- should be --second--;

at line 29, --input-should be -output--;

at line 33, --fourth-should be -second-.--; --of the second-should be -of the first--;

at line 35, --input-- should be output--;

Regarding claim 10, at line 1, "A mixer as in.." should be "The mixer circuit as in"

at line 4, –third- should be ---first—;

at line 7, -third--- should ---first---;

at line 8, ---second transistor--- should be ---first transistor---;

at line 11, --emitter--- should be ---cathode---;

at line 12, --the second--- should be ---the first---;

at line 13, ---second--- should be ---first----;

at line 14, ---the second--- should be ---the first---;

at line 16, --second--- should be ---first---;

Regarding claim 11, at line 1, "A mixer" should be "The mixer";

at line 7, ---a third resistor--- should be ---a first resistor----;

at line 10, ---third---- should be ----first----;

at line 11, ---the third---- should be ---the first----;

at line 13, ---the ground--- should be ---a ground---;

at line 14, ---fourth resistor--- should be ---second resistor---;

at line 16, ---second transistor--- should be ---first transistor---;

at line 17, --and--- should be –and an---;

at line 17, ---fourth resistor--- should be ---second resistor---;

at line 18, ---third transistor--- should be ---second transistor---;

at line 21, --fifth-- should be ---third---;

at line 22, ---transistor--- should be ---transistor,----;

at line 22, a comma is missing after ---transistor---;

at line 24, ---second-- should be ---first-- and ---third--- should be ---second---;

at line 27, --fifth-- should be --third--, and --third-- should be --second--;

at line 29, --input-should be -output--;

at line 33, --fourth-should be -second---; --of the second-should be --of the first--;

at line 35, --input-- should be -output--;

Regarding claim 12, at line 1, "A mixer" should be "The mixer";

at line 3, --the supply potential--- should be ---a supply potential---;

at line 4, ---the first input transistor--- should be --the first transistor--- to correspond with "a first transistor" of claim 15 line 7;

at line 5, ---the first terminal of the supply resistor--should be ---a first terminal of a supply resistor---, ---and to the first---- should be ---and to a first----;

at line 7, --the base-- should be --a base---;

at line 8, ---input transistor--- should be ---transistor---;

at line 9, ----the second terminal--- should be ---the first terminal---.

Regarding claim 13,

at line 14, --the first--- should be --the first input---;

at line 19, --transistor-- should be ---input transistor--.

Regarding claim 14,

at line 10, ---the RF input circuit---- should be ----the low noise RF input circuit----;

at lines 12-13, ---the emitter---- should be ---an emitter----;

at line 14 ---the base terminals--- should be ----base terminals----;

at line 16 ---the second node--- should be --a second node---;

at line 17, ---the emitter terminal---- should be ---an emitter terminal---.

Regarding claim 15,

at line 1, "A quadrature mixer" should be "The quadrature mixer circuit";

at lines 2-3, --the first capacitor-- should be --a first capacitor---, ---the first terminal of the third inductor--- should be ---a first terminal of a first inductor--- due to an inductor never being claimed priorly within the cascode circuit;

at line 6, --the first terminal--- should be --a first terminal--, --the second inductor--- should be ---a second inductor---,

at line 14, ---the first cascode--- at the end of line 14 should be ---the second cascode otherwise it would be repetitive with the previous phrase;

at line 16, --a second biasing resistor--- should be ---a first biasing resistor--- since no previous biasing resistor is claimed.

at line 17, --the first terminal--- should be --the second terminal---;

at line 18, --first bias--- should be ---second bias---;

at line 19, ---a third biasing resistor--- should be --a second biasing resistor---, and --the second bias-- should be --the first bias---;

at line 20, --the second biasing--- should be ---the first biasing---;

at line 22, --the second terminal of the third inductor--- should be --the first terminal of the first inductor---;

at line 27, ---second terminal--- should be --first terminal---.

Regarding claim 16,

at line 1, "A quadrature mixer" should be "The quadrature mixer circuit";

at line 3, --the supply potential--- should be ---a supply, potential---;

at line 4, ---the first input transistor--- should be --the first transistor--- to correspond with "a first transistor" of claim 15 line 7;

at line 5, ---the first terminal of the supply resistor--should be ---a first terminal of a supply resistor---, ---and to the first---- should be ---and to a first----;

at line 7, --the base-- should be --a base---;

at line 8, ---the first input transistor--- should be ---the first transistor---;

at line 9, ----the second terminal--- should be --the first terminal---;

Regarding claim 17,

at line 1, "A quadrature mixer" should be "The quadrature mixer circuit";

at line 2, ---the In-Phase LO drive input terminals--- should be ---In-Phase LO drive input terminals--- without the need for "a" since it is in plural form;

at lines 3-4, ---the Quadrature Phase LO drive input terminals--- should be ---Quadrature Phase LO drive input terminals--- without the need for "a" since it is in plural.

Regarding claim 18, the preamble states "A mixer circuit as in Claim 17", it should be "The quadrature mixer circuit as in claim 17", and the preamble also states --the first tracking supply--- which should be ---the first tracking supply circuit portion---- to correspond with lines 1-2 of claim 17;

at line 6, ---a third resistor--- should be ----a first resistor----;

at line 9, ---third resistor---- should be ----first resistor----;

at line 10, ---the third---- should be ---the first----;

at line 12, ---the ground--- should be ---a ground---;

at line 14, ---fourth resistor--- should be ---second resistor---;

at line 16, ---second transistor--- should be ---first transistor---;

at line 17, ---fourth resistor--- should be ---second resistor---; ---and--- should be --and an ---;

at line 19, ---third transistor--- should be ---second transistor---;

at line 22, --fifth-- should be ---third---;

at line 23, --third-- should be ---second---;

at line 26, ---second-- should be ---first--- and ---third--- should be ---second---;

at line 29, --fifth-- should be --third--, --third-- should be --second--;

at line 31, --input-- should be --output--;

at line 36, --fourth--- should be --second---; --of the second-- should be --of the first--;

at line 38, --input-- should be --output--;

at line 47, --third--- should be ---first---; ---second--- should be ---fourth---;

at line 50, ---third--- should be ---first---;

at line 51, --third--- should be ---first---;

at line 55, ---fourth resistor--- should be ---second resistor---;

at line 57, --second transistor--- should be ---first transistor---;

at line 58, --fourth--- should be ----second---; ---and--- should be --and an---;

at line 60, ---third--- should be ---second----;

at line 63, ---fifth--- should be ---third---;

at line 64, ---third--- should be ---second---;

at line 67, ---second-- should be ---first-- and ---third--- should be ---second---;

at line 70, --fifth-- should be -third--, --third-- should be -second--;

at line 72, --input-should be -output--;

at line 77, --fourth--- should be --second---; --of the second--- should be --of the first---;

at line 79, --input-- should be --output--;

Regarding claim 19, at line 1, "A quadrature mixer" should be "The quadrature mixer circuit";

at line 7, ---third--- should be ---first---;

at line 8, ---second transistor--- should be ---first transistor---;

at line 11, --emitter--- should be ---cathode---;

at line 12, --the second--- should be ---the first---;

at line 13, ---second--- should be ---first----;

at line 14, ---the second--- should be ---the first---;

at line 16, --second--- should be ---first---;

Regarding claim 20,

at line 5, --RF circuit--- should be ---RF input circuit---;

at line 6, --RF circuit--- should be ---RF input circuit---;

Regarding claim 21,

at line 7, ---low noise RF--- should be ----low noise single ended RF---;

at line 8, ---the RF input--- should be ---the low noise single ended RF input---;

at line 9, ---the RF circuit--- should be ---, the low noise single ended RF input circuit---;

at line 9, --harmonics---- should be ---harmonics,---;

at line 10, --the RF signal--- should be ---the RF input signal---.

Regarding claim 26, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 27, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 28, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 29, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 30, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 31, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 32, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 33, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Regarding claim 34, at line 1, "The mixer circuit" should be "The quadrature mixer circuit".

Appropriate correction is required or else it might lead to a 35 U.S.C. 112 2nd paragraph rejection.

Claim Objections (cont.)

6. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

There is no claim 30 in the latest preliminary amendment. Therefore misnumbered claims 31-42 been renumbered as claims 30-41.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

4. Claims 22-25 and 31-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 24 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 25 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 31 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 33 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 34 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 35 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 36 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 37 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 38 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 39 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 40 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 41 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 42 recites the limitation "the first input transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 6, 20-23 and 35-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Souetinov et al (US 6,308,058).

Regarding claim 20, Souetinov et al disclose a mixer circuit (fig. 2 and hereafter) for generating an IF output (240 & 241) responsive to an RF input (220) and an inherent LO drive source (the inherent LO drive source inputting LO signals to terminals 230, 231; col 2, lines 36-37), comprising:

a mixer core 294 having a doubly balanced mixer 207-210 including a first differentially coupled transistor pair 209 & 210 and a second differentially coupled transistor pair 207 & 208 (col 3, line 66 - col 4, line 14);

a single ended RF input circuit (290, 202, 203) coupled to receive an RF signal (at input 220; col 2, lines 45-47), the RF circuit (290, 202, 203) coupled to the mixer core, the RF circuit (290, 202, 203) including means for providing an input impedance (capacitor 272, resistor 250; col 4, lines 49-52; col 4, line 66 - col 5, line 3), means (202, 203) for splitting a phase of the RF signal (col 2, lines 30-32; col 3, lines 4-8), and means (202, 203) for decoupling noise from the RF signal to the mixer core (col 3, lines 10-14).

Regarding claim 35, Souetinov et al disclose the mixer circuit according to claim 20, wherein the first differential coupled transistor pair, the second differential coupled transistor pair and the first input transistor are all npn transistors (col 5, lines 4-11; a

typo in the reference seems to be the case with "npn bipolar resistors" which should be "npn bipolar transistors" since the reference Souetinov et al states the invention could equally be effected with pnp bipolar transistors in the cited column 5, lines 4-11).

Regarding claim 36, Souetinov et al disclose the mixer circuit according to claim 20, wherein the first differential coupled transistor pair, the second differential coupled transistor pair and the first input transistor are all pnp transistors (column 5, lines 4-11).

Regarding claim 6, Souetinov et al disclose a mixer circuit (fig. 2) for generating an IF output 240, 241 responsive to an RF input 220 and an inherent LO drive source LO inputting signals 230, 231 (col 2, lines 36-37), comprising:

a mixer core 294 having a doubly balanced mixer including a first differentially coupled transistor pair 207, 208 and a second differentially coupled transistor 209, 210, the mixer core 294 coupled to receive a LO drive signal (230, 231), the LO drive signal having a plurality of harmonics (col 4, lines 23-25);

a low noise RF input circuit 290 coupled to the mixer core 294 through a folded cascode circuit 202, 203 (col 3, lines 21-23), wherein the cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of harmonics (col 4, 20-41).

Regarding claim 21, Souetinov et al disclose a mixer circuit (fig. 2 and hereafter) for generating an IF output (240, 241) responsive to an RF input (220) and an inherent LO drive source (inputting LO signals to terminals 230 & 231; col 2, lines 33-37), comprising:

a mixer core (294) having a doubly balanced mixer (207-210) including a first differentially coupled transistor pair (209 & 210) and a second differentially coupled transistor pair (207 & 208) (col 3, line 66 - col 4, line 14; abstract, lines 5-6), the mixer core (294) coupled to receive a LO drive signal (230, 231), the LO drive signal (230, 231) having a plurality of harmonics (col 4, lines 20-41 „ col 2, lines 32-57);

a low noise single ended RF input circuit (290) coupled to the mixer core (294) through a cascode circuit (202-203) (col 3, lines 10-14; col 2, lines 45-54),

the cascode circuit (202, 203) further isolates the RF input circuit from the LO drive signal; the low noise RF input circuit (290) coupled to receive an RF input signal (220), the RF circuit including means (250 & 272) for providing an input impedance (col 4, lines 49-52; col 4, line 66 - col 5, line 3) and means (202 & 203 at phase splitter stage 292) for splitting a phase of the RF signal (col 2, lines 48-60; col 3, lines 4-8).

Regarding claim 22, Souetinov et al disclose the mixer circuit according to claim 6 wherein Souetinov et al further disclose:

the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor may be npn transistors (npn bipolar transistors; col 5, lines 4-11; a typo in the reference appears to be the case with "npn bipolar resistors" which should be "npn bipolar transistors" since the reference Souetinov et al states the invention could equally be effected with pnp bipolar transistors in the cited column 5, lines 4-11).

Regarding claim 23, Souetinov et al disclose the mixer circuit according to claim 6 wherein Souetinov et al further disclose: the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor may be pnp transistors (pnp bipolar transistors; col 5, lines 4-11).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 24, 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Souetinov et al (US 6,308,058).

Regarding claim 24, Souetinov et al disclose the mixer circuit according to claim 6 wherein Souetinov et al further disclose:

the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all FET transistors (field effect transistors; col 5, lines 4-11).

Souetinov et al don't specifically disclose:

the FET transistors are MOSFET transistors. However, it is well known in the art that MOSFET transistors are one type of FET transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically use MOSFET transistors in order to minimize the effect of any differential offset currents and to reduce power losses.

Regarding claim 37, Souetinov et al disclose the mixer circuit according to claim 20, wherein Souetinov et al further disclose the first differential coupled transistor

pair, the second differential coupled transistor pair and the first input transistor are all FET transistors (field effect transistors; column 5, lines 4-11). Souetinov et al do not specifically disclose: the FET transistors are MOSFET transistors. However, it is well known in the art that a MOSFET transistor is one type of FET transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically use MOSFET transistors in order to minimize the effect of any differential offset currents and to save power.

Regarding claim 38, Souetinov let al disclose the mixer circuit according to claim 20, wherein Souetinov et al further disclose the first differential coupled transistor pair, the second differential coupled transistor pair and the first input transistor are all FET transistors (field effect transistors; see col 5, lines 4-11).

Souetinov et al do not specifically disclose: the FET transistors are all MESFET transistors. However, it is well known in the art that a MESFET transistor is one type of FET transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically use a MESFET transistor as one type of FET transistors of Souetinov et al in order to reduce distortion into the system due to its almost perfect square law characteristics.

Allowable Subject Matter

12. Independent claims 1, 13, and 14 would be allowable over the cited prior art if rewritten to overcome the claim objections above.

Regarding claim 1, Souetinov et al disclose a mixer circuit for generating an IF output responsive to an RF input (220) and an inherent LO drive source (inputting LO drive signals to terminals 230 & 231), comprising:

a mixer core (292) having a doubly balanced mixer including a first differentially coupled transistor pair (209 & 210) and a second differentially coupled transistor pair (207 & 208);

an RF input circuit (290) coupled to the mixer core (292), the RF input circuit comprising:

an input inductor (280) having a first terminal and a second terminal.

However, the cited prior art fails to further disclose:

the input inductor having a first terminal coupled to receive an RF input signal and a second terminal;

a biasing resistor having a first terminal coupled to the second terminal of the input inductor and a second terminal coupled to a first bias voltage;

a first input transistor having a control terminal coupled to the second terminal of the input inductor, a second terminal, and a third terminal; a second inductor having a first terminal coupled to the second terminal of the first input transistor and to the first differentially coupled transistor pair, the second inductor also having a second terminal coupled to a ground potential; a supply resistor having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to a supply potential; a first capacitor having a first terminal also coupled to the second terminal of the first input transistor and a second terminal coupled to the

second differentially coupled transistor pair; and a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

Regarding claim 13, Souetinov et al disclose a quadrature mixer circuit (fig. 2) for generating a quadrature IF output (at output 240, 241, 242, 243) responsive to an RF input 220 and a quadrature pair of LO drive signals 230, 231, 232, 233 comprising: a mixer core 294, 295 having a first doubly balanced mixer 294 including a first differentially coupled transistor pair 207, 208 and a second differentially coupled transistor pair 209, 210 and a second doubly balanced mixer 295 including a third differentially coupled transistor pair 211, 212 and a fourth differentially coupled transistor pair 213, 214; an RF input circuit 290 coupled to the mixer core via 292, the RF input circuit comprising: a first input transistor 201 having a base terminal, an emitter terminal, and a collector terminal; a second inductor 280 having a first terminal coupled to the emitter of the first transistor 201; the second inductor 280 also having a second terminal coupled to a ground potential (col 2, lines 52-54); a resistor 250 having a first terminal coupled to the collector of the first input transistor 201; a first capacitor 272 having a first terminal also coupled to the collector of the first input transistor 201.

However, the cited prior art fail to disclose:

the RF input circuit further comprising:

an input inductor having a first terminal coupled to receive an RF input signal and a second terminal; a biasing resistor having a first terminal coupled to the second

terminal of the input inductor and a second terminal coupled to a first bias voltage; the first input transistor having the base terminal coupled to the second terminal of the input inductor; the second inductor having the first terminal coupled to the first differentially coupled transistor pair and to the third differentially coupled transistor pair, a supply resistor having a first terminal coupled to the collector of the first transistor and a second terminal coupled to a supply potential;

a first capacitor having a first terminal also coupled to the collector of the first transistor and a second terminal coupled to the second differentially coupled transistor pair and to the fourth differentially coupled transistor pair; and a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

Regarding claim 14, Souetinov et al disclose a quadrature mixer circuit (fig. 2) for generating an IF output (240, 241) responsive to an RF input (220) and a quadrature pair of LO drive signals (230,231 and 232,233) (col 2, lines 36-37), comprising:

a mixer core (294, 295; fig. 2 and hereafter) having a first doubly balanced mixer 207-210 including a first differentially coupled transistor pair 209 & 210 and a second differentially coupled transistor pair 207 & 208 (col 3, line 66 - col 4, line 14), and having a second doubly balanced mixer (211-214) including a third differentially coupled transistor pair (213-214) and a second differentially coupled transistor pair 211-212 (col 3, line 66 - col 4, line 14),

the mixer core (294, 295) coupled to receive a quadrature LO drive signal (230, 231, 232, 233), the quadrature LO drive signal having a plurality of harmonics (col 4, lines 20-41; col 2, lines 32-57);

a low noise RF input circuit (290; col 3, lines 21-23) coupled to the mixer core (294, 295) through a folded cascode circuit (202-203; col 2, lines 48-50, col 3, lines 10-

14. Claims 15 and 16 would be allowable if rewritten to overcome the drawing objection and the claim objection set forth in this Office action and to include all of the limitations of the base claim, the base claim also rewritten to overcome the claim objections, and any intervening claims, the intervening claims also rewritten to overcome the claim objections.

15. Dependent claims 7-12, 17-19, 26-29 would be allowable if rewritten to overcome the claim objections set forth in this Office action and to include all of the limitations of the base claim, the base claim also rewritten to overcome the claim objections, and any intervening claims, the intervening claims also rewritten to overcome the claim objections.

Regarding claim 7, Souetinov et al disclose a mixer as in claim 6 wherein the folded cascode circuit (fig. 2) comprises:

a first cascode transistor (203) having a collector terminal coupled to the second differentially coupled transistor pair (209, 210) and a base terminal (see figure), a second cascode transistor (202) having a base terminal coupled to the base terminal of the first cascode transistor (203), the first cascode transistor having an emitter terminal. However, Souetinov et al and the cited prior art fail to disclose the folded cascode circuit further comprises:

the first cascode transistor having an emitter terminal coupled to a second terminal of a first capacitor and to a first terminal of a third inductor,

the second cascode transistor having an emitter terminal coupled to a first terminal of a second inductor and to an emitter terminal of a first transistor, and a collector terminal coupled to the first differentially coupled transistor pair,

a second capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to a second terminal of the first capacitor, the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the first cascode transistor and a second terminal coupled to the second terminal of the second capacitor, a second biasing resistor having a first terminal coupled to the first terminal of the second capacitor and a second terminal coupled to a second bias voltage.

Regarding claim 11, Souetinov et al and Chen et al disclose a mixer circuit as in claim 6, wherein the cited prior art fail to disclose: the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising: a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal, a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal, a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal, a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential, a loop amplifier having a first terminal coupled to the

second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal, a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal, a second transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupler to receive a first: LO drive signal and emitter terminal, a third transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second transistor and a collector terminal, a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third transistor; a second current supply having a first terminal coupled to the emitter terminal of the second transistor and to the emitter terminal of the third transistor and a second terminal coupled to the ground potential, a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input, a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential, a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input, a fourth current supply having a first

terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

Regarding claim 12, Souetinov et al and Chen et al disclose a mixer circuit as in claim 6, wherein the cited prior art fails to further disclose the low noise RF input circuit further includes an RF feedback circuit coupled to the RF input circuit, the RF feedback circuit comprising: a second transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor, a feedback resistor, having a first terminal coupled to the base terminal of the first input transistor and a second terminal, a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

16. Claims 31-34 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set: forth in this Office action and also if rewritten to overcome the claim objections above and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N Le whose telephone number is (703) 308-5836. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lana Le

November 12, 2004